ABSTRACT OF THE DISCLOSURE

A multi-chip package device includes package terminals, a semiconductor memory chip and an interface chip. The semiconductor memory chip has a test circuit and a test terminal. The test circuit is enabled when a high voltage level is applied to the test terminal. The interface chip is connected to the package terminals and the semiconductor memory. The interface chip includes a control circuit, a high voltage generating circuit and a transferring circuit. The control circuit has memory terminals connected to the package terminals. The control circuit generates a test signal and an enable signal in response to signals received from the memory terminals. The high voltage generating circuit generates a high voltage signal having the high voltage level in response to the enable signal. The transferring circuit provides the high voltage signal to the memory chip in response to the test signal.